What Is Claimed Is:

1. A method, comprising:

receiving a function in assembly code;

parsing said function into a parsed group selected from a group consisting of an instruction, data, a constant, a coefficient, and a factor;

converting one or more of said parsed group into one or more operation codes, wherein an operation code is a numeric representation for each of said parsed group;

determining said one or more operation codes to be executed on a processing element;

combining said one or more operation codes into a file; and

converting said file into a state machine representation.

2. The method of claim 1, said converting said file into a state machine representation further comprises:

assigning each of said one or more operation codes a state, wherein an output of said state is an operation number;

determining a next state for each of said one or more operation codes, wherein said next state is a function of said state and an input signal;

associating said operation number with a reconfigurator vector; and

generating a state equation for each state.

3. The method of claim 2, further comprising:

mapping said state equations to a control unit reconfigurable logic array; and

programming a fuse map for said control unit reconfigurable logic array.

4. The method of claim 3, further comprising:

producing an output reconfigurator vector look-up table, wherein said reconfigurator vector look-up table converts said operation number to a reconfigurator vector.

5. The method of claim 4, further comprising:

creating a configuration packet;

downloading said configuration packet to said processing element; and

programming said processing element with said configuration packet.

6. The method of claim 5, wherein said configuration packet includes data selected from a group consisting of said fuse map, said output reconfigurator vector look-up table, said parsed group, one or more fuse maps for other control unit reconfigurable logic arrays, routing information, one or more processing element addresses, and packet sizes.

7. The method of claim 1, wherein said processing element includes as least one micro-coded accelerator.

8. A machine-readable medium that provides instructions, which when executed by a computing platform, cause said computing platform to perform operations comprising a method of:

receiving a function in assembly code;

parsing said function into a parsed group selected from a group consisting of an instruction, data, a constant, a coefficient, and a factor;

converting one or more of said parsed group into one or more operation codes, wherein an operation code is a numeric representation for each of said parsed group;

determining said one or more operation codes to be executed on a processing element;

combining said one or more operation codes into a file; and

converting said file into a state machine representation.

9. The machine-readable medium of claim 8, providing further instructions, which when executed by a computing platform, cause the computing platform to perform a further operation of:

assigning each of said one or more operation codes a state, wherein an output of said state is an operation number;

determining a next state for each of said one or more operation codes, wherein said next state is a function of said state and an input signal;

associating said operation number with a reconfigurator vector; and

generating a state equation for each state.

10. The machine-readable medium of claim 9, providing further instructions, which when executed by a computing platform, cause the computing platform to perform a further operation of:

mapping said state equations to a control unit reconfigurable logic array; and

programming a fuse map for said control unit reconfigurable logic array.

11. The machine-readable medium of claim 10, providing further instructions, which when executed by a computing platform, cause the computing platform to perform a further operation of:

producing an output reconfigurator vector look-up table, wherein said reconfigurator vector look-up table converts said operation number to a reconfigurator vector.

12. The machine-readable medium of claim 11, providing further instructions, which when executed by a computing platform, cause the computing platform to perform a further operation of:

creating a configuration packet;

downloading said configuration packet to said processing element; and

programming said processing element with said configuration packet.

13. The machine-readable medium of claim 12, wherein said configuration packet includes data selected from a group consisting of said fuse map, said output reconfigurator vector look-up table, said parsed group, one or more fuse maps for other control unit reconfigurable logic arrays, routing information, one or more processing element addresses, and packet sizes.

14. The machine-readable medium of claim 8, wherein said processing element includes as least one micro-coded accelerator.

15. A system, comprising:

an instruction converter to receive a function in assembly code and to parse said function into a parsed group selected from the group consisting of an instruction, data, a constant, a coefficient, and a factor;

said instruction converter to convert said parsed group into one or more operation codes, wherein each of said operation codes is a numeric representation for each selection of said parsed group;

a processing element combiner to determine said one or more operation codes to be executed on a processing element and combine said one or more operation codes into a file; and

a state equation generator to convert said file into a state machine representation.

16. The system of claim 15, further comprising:

said instruction converter (i) to assign an operation number as an output of a state of said one or more operation codes, (ii) to determine a next state for each of said one or more operation codes, wherein said next state is a function of said state and an input signal, (iii) to associate said operation number with a reconfigurator vector, and (iv) to generate a state equation for each state.

17. The system of claim 16, further comprising:

a reconfigurable logic array configurator to map said state equations to a control unit reconfigurable logic array, and program a fuse map for said control unit reconfigurable logic array.

18. The system of claim 17, further comprising:

a reconfigurator vector look-up table to produce an output reconfigurator vector look-up table, said reconfigurator vector look-up table to convert said operation number to a reconfigurator vector.

19. The system of claim 18, further comprising:

a configuration packet generator to create a configuration packet and to program said processing element with said configuration packet.

20. The system of claim 19, wherein said configuration packet includes data selected from a group consisting of said fuse map, said output reconfigurator vector look-up table, said parsed group, one or more fuse maps for other control

unit reconfigurable logic arrays, routing information, one or more processing element addresses, and packet sizes.

21. The system of claim 15, wherein said processing element includes as least one micro-coded accelerator.